REMARKS

Applicant respectfully traverses and requests reconsideration.

Claims 1, 6, 7, 17, and 19 are amended.

Claims 6 and 9 stand objected to due to informalities. Claims 6 and 9 have been amended to correct the informalities noted by the Examiner.

Claims 1-4 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication 20040103272 to Zimmer. The Zimmer reference is drawn to a method for using a processor cache as a RAM during system initialization. Zimmer teaches storing and retrieving initial contents of the initialization process and/or early firmware code via a processor cache prior to availability of system memory. The cache is used by the processor as a pre-memory heap and stack space during initialization. However, Zimmer does not teach using a second processor, such as a graphics processor or other processor, to execute memory initialization and sizing using data in the processor cache.

The method for basic input output system loading for a personal computer of Applicant's Claim 1 is amended such that the step of "executing a memory initialization and sizing operation using the data in the cache memory" includes "using a second processor operatively coupled to the central processing unit." This feature is not taught or contemplated by Zimmer. Therefore, Applicant's claimed invention, as recited in Claim 1, is not anticipated by Zimmer. Claims 2-4 comprise patentably distinct further limitations on claim 1 that should likewise be in condition for allowance.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zimmer as applied above to claim 1 above and further in view of Lo et al. (US Patent 4,922,451). In regards to claim 5, Applicant references the relevant remarks under claims 1-4 above wherein Zimmer

fails to disclose at least one feature of base claim 1, that of executing a memory initialization and sizing operation using the processor cache on a first processor and a second processor. The additional reference of Lo et al. is directed to a microcomputer system with a memory remapping capability. While Lo et al. discuss memory sizing, they do not teach or suggest executing a memory initialization and sizing operation using a cache of one processor in conjunction with a second processor. Neither Zimmer nor Lo et al. nor the combination of these references teach or suggest at least this feature of claim 1 and of dependent claim 5.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zimmer as applied to claim 1 above and further in view of Gammel et al. (US Patent Publication 20030005314). In regards to claim 6, Applicant references the relevant remarks under claims 1-4 above wherein Zimmer fails to disclose at least one feature of base claim 1, that of executing a memory initialization and sizing operation using the processor cache on a first processor and a second processor. The additional reference of Gammel et al. is directed to a microprocessor having a processing unit 2 and a cache 8 where the cache temporarily stores encrypted data. While Gammel et al. describe flushing and initializing a cache, they do not teach or suggest using a cache of one processor in conjunction with a second processor to execute a memory initialization and sizing operation. Neither Zimmer nor Gammel et al. nor the combination of these references teach or suggest at least this feature of claim 1 and of dependent claim 6.

Claims 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zimmer as applied to claim 1 above and further in view of Polyudov (US Patent Publication 20040186988). In regards to claim 7-8, Applicant references the relevant remarks under claims 1-4 above wherein Zimmer fails to disclose at least one feature of base claim 1, that of executing a memory initialization and sizing operation using the processor cache on a first processor and a

second processor. The additional reference of Polyudov is directed to a system having multiple processors 4A-4D to 6A-6D. All the processors share a common RAM 10. One of the processors acts as a boot processor for the system. The boot processor passes updated boot initialization data to other processors using the common RAM 10. While Polyudov describes a system having more that one processor, the reference does not teach or suggest using a cache of one processor in conjunction with a second processor to execute a memory initialization and sizing operation. Neither Zimmer nor Polyudov nor the combination of these references teach or suggest at least this feature of claim 1 and of dependent claims 7-8.

Claims 9-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Polyudov in view of Zimmer. In regards to claims 9-13, Applicant references the relevant remarks under claims 1-4 and 7-8 above. While Zimmer describes a processor having a cache, it does not teach or suggest another processor writing to this cache prior to startup operations of the processor that wrote the data. While Polyudov describes a system having multiple processors, it does not teach or suggest another processor writing to this cache as claimed. Therefore, the references, taken separately or in combination, do not teach at least the feature of claim 9 of "the graphics processor writing data to the cache memory (on the central processing unit) prior to the start-up operations." Therefore, claim 9, and depending claims 10-13 are not unpatentable over Polyudov in view of Zimmer.

Claims 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Polyudov in view of Zimmer, as applied to claim 9 above and further in view of Gammel et al. In regards to claims 14-16, Applicant references the relevant remarks under claims 10-13 above. While the reference of Gammel et al. is directed to a microprocessor having a processing unit 2 and a cache 8 where the cache temporarily stores encrypted data, it does not teach or suggest

another processor writing to this cache. Therefore, the references, taken separately or in combination, do not teach at least the feature of claim 9 of "the graphics processor writing data to the cache memory (on the central processing unit) prior to the start-up operations." Therefore, claim 9, and depending claims 14-16, are not unpatentable over Polyudov in view of Zimmer and further in view of Gammel et al.

Claims 17-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zimmer in view of Gammel. In regards to claims 17-20, Applicant references the relevant remarks under claims 1-4 and 6 above. A method for basic input output system loading in a graphics processor of Applicant's Claim 17 is amended such that the step of "executing a plurality of executable instructions" is performed "using the cache memory (in a central processing unit) and a second processor." While Zimmer describes a processor having a cache, it does not teach or suggest another processor writing to this cache. While the reference of Gammel et al. is directed to a microprocessor having a processing unit 2 and a cache 8 where the cache temporarily stores encrypted data, it does not teach or suggest another processor writing to this cache. Therefore, the references, taken separately or in combination, do not teach at least the feature of claim 17 of "executing a plurality of executable instructions using the cache memory (in a central processing unit) and a second processor." Therefore, claim 17, and depending claims 18-20, are not unpatentable over Zimmer in view of Gammel.

New claim 21 is believed to be allowable as the cited references do not appear to teach or suggest utilizing cache memory among a plurality of processors as claimed.

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited

to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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